

VERILOG PROJECT

VEDIC MULTIPLIER ✕



8-Bit Multiplier

```
module veda_8bits_8x8 {
    input [7:0]a;
    input [7:0]b;
    output [15:0]c;

    wire [15:0]p0;
    wire [15:0]p1;
    wire [15:0]p2;
    wire [15:0]p3;
    wire [15:0]p4;
    wire [15:0]p5;
    wire [15:0]p6;
    wire [15:0]p7;
    wire [15:0]p8;
    wire [15:0]p9;
    wire [15:0]p10;
    wire [15:0]p11;
    wire [15:0]p12;
    wire [15:0]p13;
    wire [15:0]p14;
    wire [15:0]p15;

    veda_8x8_0 a,b,p0,p1,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;
    veda_8x8_1 a,b,p1,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;
    veda_8x8_2 a,b,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;
    veda_8x8_3 a,b,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;

    assign temp0 = (a[7]&b[7])<16;
    add_8_bits temp0[15:0],temp0[15:0];
    assign temp1 = (a[7]&b[6])<15;
    assign temp2 = (a[7]&b[5])<14;
    assign temp3 = (a[7]&b[4])<13;
    add_16_bits temp0,temp1,temp2,temp3;
    assign temp4 = (a[7]&b[3])<12;
    add_16_bits temp4,temp4,temp4,temp4;

    add_16_bits temp4,temp4,temp4,temp4;

    assign c[15:0] = temp4;
    assign c[15:0] = temp4;
endmodule
```

(Code for 8 bit multiplier)

4-Bit Multiplier

```
module veda_4x4_4bits_4x4 {
    input [3:0]a;
    input [3:0]b;
    output [7:0]c;

    wire [7:0]p0;
    wire [7:0]p1;
    wire [7:0]p2;
    wire [7:0]p3;
    wire [7:0]p4;
    wire [7:0]p5;
    wire [7:0]p6;
    wire [7:0]p7;
    wire [7:0]p8;
    wire [7:0]p9;
    wire [7:0]p10;
    wire [7:0]p11;
    wire [7:0]p12;
    wire [7:0]p13;
    wire [7:0]p14;
    wire [7:0]p15;

    veda_4x4_0 a,b,p0,p1,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;
    veda_4x4_1 a,b,p1,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;
    veda_4x4_2 a,b,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;
    veda_4x4_3 a,b,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;

    assign temp1 = (a[3]&b[3])<8;
    add_4_bits temp1[7:0],temp1[7:0];
    assign temp2 = (a[3]&b[2])<7;
    assign temp3 = (a[3]&b[1])<6;
    add_4_bits temp1,temp2,temp3,temp3;

    assign temp4 = (a[3]&b[0])<3;
    add_4_bits temp4,temp4,temp4,temp4;
    assign c[7:0] = temp4;
endmodule
```

(Code for 4 bit multiplier)

```
0 = 00000000, 0=00000000, --- = 0000000000000000
100 = 00000100, 0=00000000, --- = 0000000000000000
100 = 00000100, 0=00000000, --- = 0000000000000000
100 = 00000100, 0=00000000, --- = 0000000000000000
100 = 00000100, 0=00000000, --- = 0000000000000000
100 = 00000100, 0=00000000, --- = 0000000000000000
```

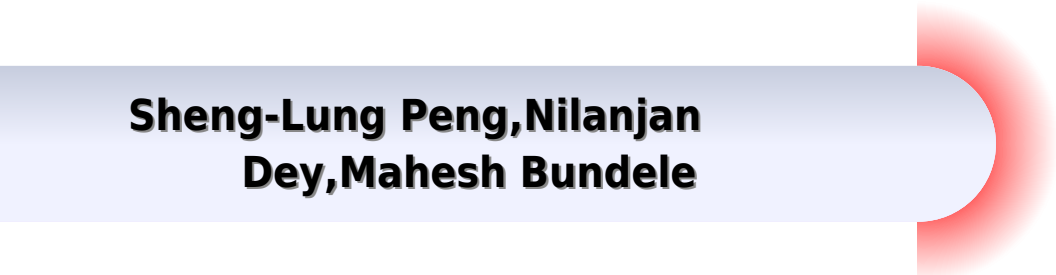
(c gives the multiplication of a and b)



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Advanced Digital System Design Shirshendu Roy, 2023-09-25 The book is designed to serve as a textbook for courses offered to undergraduate and graduate students enrolled in electrical electronics and communication engineering The objective of this book is to help the readers to understand the concepts of digital system design as well as to motivate the students to pursue research in this field Verilog Hardware Description Language HDL is preferred in this book to realize digital architectures Concepts of Verilog HDL are discussed in a separate chapter and many Verilog codes are given in this book for better understanding Concepts of system Verilog to realize digital hardware are also discussed in a separate chapter The book covers basic topics of digital logic design like binary number systems combinational circuit design sequential circuit design and finite state machine FSM design The book also covers some advanced topics on digital arithmetic like design of high speed adders multipliers dividers square root circuits and CORDIC block The readers can learn about FPGA and ASIC implementation steps and issues that arise at the time of implementation One chapter of the book is dedicated to study the low power design techniques and another to discuss the concepts of static time analysis STA of a digital system Design and implementation of many digital systems are discussed in detail in a separate chapter In the last chapter basics of some advanced FPGA design techniques like partial re configuration and system on chip SoC implementation are discussed These designs can help the readers to design their architecture This book can be very helpful to both undergraduate and postgraduate students and researchers

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Jyothi M. Shirur, Rekha P., 2013-07-10 This book is a collection of papers presented by renowned researchers keynote speakers and academicians in the International Conference on VLSI Communication Analog Designs Signals Systems and Networking VCASAN 2013 organized by B N M Institute of Technology Bangalore India during July 17 19 2013 The book provides global trends in cutting edge technologies in electronics and communication engineering The content of the book is useful to engineers researchers and academicians as well as industry professionals

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