Verification Methodology Manual for Low Power

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Verification Methodology Manual For Low Power:

Verification Methodology Manual for Low Power Srikanth Jadcherla,2009-01-01 *ESL Models and their Application* Brian Bailey,Grant Martin,2009-12-15 This book arises from experience the authors have gained from years of work as industry practitioners in the field of Electronic System Level design ESL At the heart of all things related to Electronic Design Automation EDA the core issue is one of models what are the models used for what should the models contain and how should they be written and distributed Issues such as interoperability and tool transportability become central factors that may decide which ones are successful and those that cannot get sufficient traction in the industry to survive Through a set of real examples taken from recent industry experience this book will distill the state of the art in terms of System Level Design models and provide practical guidance to readers that can be put into use This book is an invaluable tool that will aid readers in their own designs reduce risk in development projects expand the scope of design projects and improve developmental processes and project planning **Low Power Methodology Manual** David Flynn,Rob Aitken,Alan Gibbons,Kaijian Shi,2007-07-31 Tools alone aren t enough to reduce dynamic and leakage power in complex chip designs a well planned methodology is needed Following in the footsteps of the successful Reuse Methodology Manual RMM authors from ARM and Synopsys have written this Low Power Methodology Manual LPMM to describe such a low power methodology with a practical step by step approach Richard Goering Software Editor EE Times Excellent compendium of low power techniques and guidelines with balanced content spanning theory and practical implementation The LPMM is a very welcome addition to the field of low power SoC implementation that has for many years operated in a largely ad hoc fashion Sujeeth Joseph Chief Architect Semiconductor and Systems Solutions Unit Wipro Technologies The LPMM enables broader adoption of aggressive power management techniques based on extensive experience and silicon example with real data that every SOC designer can use to meet the difficulties faced in managing the power issues in deep submicron designs Anil Mankar Sr VP Worldwide Core Engineering and Chief Development Officer Conexant Systems Inc Managing power at 90nm and below introduces significant challenges to design flow The LPMM is a timely and immediately useful book that shows how combination of tools IP and methodology can be used together to address power management Nick Salter Head of Chip Integration CSR plc FPGA-based Prototyping Methodology Manual Doug Amos,Austin Lesea,Rene Richter,2011 This book collects the best practices FPGA based Prototyping of SoC and ASIC devices into one place for the first time drawing upon not only the authors own knowledge but also from leading practitioners worldwide in order to present a snapshot of best practices today and possibilities for the future The book is organized into chapters which appear in the same order as the tasks and decisions which are performed during an FPGA based prototyping project We start by analyzing the challenges and benefits of FPGA based Prototyping and how they compare to other prototyping methods We present the current state of the available FPGA technology and tools and how to get started on a project The FPMM also compares between home made and

outsourced FPGA platforms and how to analyze which will best meet the needs of a given project The central chapters deal with implementing an SoC design in FPGA technology including clocking conversion of memory partitioning multiplexing and handling IP amongst many other subjects The important subject of bringing up the design on the FPGA boards is covered next including the introduction of the real design into the board running embedded software upon it in and debugging and iterating in a lab environment Finally we explore how the FPGA based Prototype can be linked into other verification methodologies including RTL simulation and virtual models in SystemC Along the way the reader will discover that an adoption of FPGA based Prototyping from the beginning of a project and an approach we call Design for Prototyping will greatly increase the success of the prototype and the whole SoC project especially the embedded software portion Design for Prototyping is introduced and explained and promoted as a manifesto for better SoC design Readers can approach the subjects from a number of directions Some will be experienced with many of the tasks involved in FPGA based Prototyping but are looking for new insights and ideas others will be relatively new to the subject but experienced in other verification methodologies still others may be project leaders who need to understand if and how the benefits of FPGA based prototyping apply to their next SoC project We have tried to make each subject chapter relatively standalone or where necessary make numerous forward and backward references between subjects and provide recaps of certain key subjects We hope you like the book and we look forward to seeing you on the FPMM on line community soon go to www synopsys com fpmm

Low-Power Wireless Communication Circuits and Systems Kiat Seng Yeo,Kaixue Ma,2018-05-03 The increasing demand for extremely high data rate communications has urged researchers to develop new communication systems Currently wireless transmission with more than one Giga bits per second Gbps data rates is becoming essential due to increased connectivity between different portable and smart devices To realize Gbps data rates millimeter wave MMW bands around 60 GHz is attractive due to the availability of large bandwidth of 9 GHz Recent research work in the Gbps data rates around 60 GHz band has focused on short range indoor applications such as uncompressed video transfer high speed file transfer between electronic devices and communication to and from kiosk Many of these applications are limited to 10 m or less because of the huge free space path loss and oxygen absorption for 60 GHz band MMW signal This book introduces new knowledge and novel circuit techniques to design low power MMW circuits and systems It also focuses on unlocking the potential applications of the 60 GHz band for high speed outdoor applications The innovative design application significantly improves and enables high data rate low cost communication links between two access points seamlessly The 60 GHz transceiver system on chip provides an alternative solution to upgrade existing networks without introducing any building renovation or external network laying works **Low-Power Processors and Systems on Chips** Christian Piguet,2018-10-03 The power consumption of microprocessors is one of the most important challenges of high performance chips and portable devices In chapters drawn from Piguet s recently published Low Power Electronics Design this volume

addresses the design of low power microprocessors in deep submicron technologies It provides a focused reference for specialists involved in systems on chips from low power microprocessors to DSP cores reconfigurable processors memories ad hoc networks and embedded software Low Power Processors and Systems on Chips is organized into three broad sections for convenient access The first section examines the design of digital signal processors for embedded applications and techniques for reducing dynamic and static power at the electrical and system levels The second part describes several aspects of low power systems on chips including hardware and embedded software aspects efficient data storage networks on chips and applications such as routing strategies in wireless RF sensing and actuating devices The final section discusses embedded software issues including details on compilers retargetable compilers and coverification tools Providing detailed examinations contributed by leading experts Low Power Processors and Systems on Chips supplies authoritative information on how to maintain high performance while lowering power consumption in modern processors and SoCs It is a must read for anyone designing modern computers or embedded systems Low-Power Electronics Design Christian Piguet,2018-10-03 The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high performance chips and portable devices The study of power saving design methodologies now must also include subjects such as systems on chips embedded software and the future of microelectronics Low Power Electronics Design covers all major aspects of low power design of ICs in deep submicron technologies and addresses emerging topics related to future design This volume explores in individual chapters written by expert authors the many low power techniques born during the past decade It also discusses the many different domains and disciplines that impact power consumption including processors complex circuits software CAD tools and energy sources and management The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality They investigate nanotechnologies optical circuits ad hoc networks e textiles as well as human powered sources of energy Low Power Electronics Design delivers a complete picture of today s methods for reducing power and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now *Better Software. Faster!* Tom De Schutter,2014-03-17 The recent rise of smart products has been made possible through tight co design of hardware and software The growing amount of software and hence processors in applications all around us allows for increased flexibility in the application functionality through its life cycle Not so long ago a device felt outdated after you owned it for a couple of months Today a continuous stream of new software applications and updates make products feel truly smart The result is an almost magical user experience where the same product can do more today than it could do yesterday In this book we dive deep into a key methodology to enable concurrent hardware software development by decoupling the dependency of the software development from hardware availability virtual prototyping The ability to start software development much earlier in the design cycle drives a true shift left of the entire product development schedule and results in better products that are

available earlier in the market Throughout the book case studies illustrate how virtual prototypes are being deployed by major companies around the world If you are interested in a quick feel for what virtual prototyping has to offer for practical deployment we recommend picking a few case studies to read before diving into the details of the methodology Of course this book can only offer a small snapshot of virtual prototype use cases for faster software development However as most software bring up debug and test principles are similar across markets and applications it is not hard to realize why virtual prototypes are being leveraged whenever software is an intrinsic part of the product functionality after reading this book

Computer Aided Verification Aarti Gupta,Sharad Malik,2008-06-17 This book constitutes the refereed proceedings of the 20th International Conference on Computer Aided Verification CAV 2008 held in Princeton NJ USA in July 2008 The 33 revised full papers presented together with 14 tool papers and 2 invited papers and 4 invited tutorials were carefully reviewed and selected from 104 regular paper and 27 tool paper submissions The papers are organized in topical sections on concurrency memory consistency abstraction refinement hybrid systems dynamic verification modeling and specification formalisms decision procedures program verification program and shape analysis security and program analysis hardware verification model checking space efficient algorithms and model checking *The Ten Commandments for Effective Standards* Karen Bartleson,Rick Jamison,2010 Computer chip industry veteran Bartleson provides ideas for creating better standards increasing respect for the standardization process and ways for leveraging others industry expertise to create more effective technical standards **Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation** Jose L. Ayala,Braulio Garcia-Camara,Manuel Prieto,Martino Ruggiero,Gilles Sicard,2011-09-15 This book constitutes the refereed proceedings of the 21st International Conference on Integrated Circuit and System Design PATMOS 2011 held in Madrid Spain in September 2011 The 34 revised full papers presented were carefully reviewed and selected from numerous submissions The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems and focus especially on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling design characterization analysis and optimization **Reuse Methodology Manual** Pierre Bricaud,2012-12-06 Silicon technology now allows us to build chips consisting of tens of millions of transistors This technology not only promises new levels of system integration onto a single chip but also presents significant challenges to the chip designer As a result many ASIC developers and silicon vendors are re examining their design methodologies searching for ways to make effective use of the huge numbers of gates now available These designers see current design tools and methodologies as inadequate for developing million gate ASICs from scratch There is considerable pressure to keep design team size and design schedules constant even as design complexities grow Tools are not providing the productivity gains required to keep pace with the increasing gate counts available from deep submicron technology Design reuse the use of pre designed and pre verified cores is the most promising

opportunity to bridge the gap between available gate count and designer productivity Reuse Methodology Manual for System On A Chip Designs Second Edition outlines an effective methodology for creating reusable designs for use in a System on a Chip SoC design methodology Silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem Instead this manual is an attempt to capture and incrementally improve on current best practices in the industry and to give a coherent integrated view of the design process Reuse Methodology Manual for System On A Chip Designs Second Edition will be updated on a regular basis as a result of changing technology and improved insight into the problems of design reuse and its role in producing high quality SoC designs Reuse Methodology Manual for System-On-A-Chip Designs Pierre Bricaud,2013-03-09 Silicon technology now allows us to build chips consisting of tens of millions of transistors This technology promises new levels of system integration onto a single chip but also presents significant challenges to the chip designer As a result many ASIC developers and silicon vendors are re examining their design methodologies searching for ways to make effective use of the huge numbers of gates now available These designers see current design tools and methodologies as inadequate for developing million gate ASICs from scratch There is considerable pressure to keep design team size and design schedules constant while design complexities grow Tools are not providing the productivity gains required to keep pace with the increasing gate counts available from deep submicron technology Design reuse the use of pre designed and pre verified cores is the most promising opportunity to bridge the gap between available gate count and designer productivity Reuse Methodology Manual for System On A Chip Designs outlines an effective methodology for creating reusable designs for use in a System on a Chip SoC design methodology Silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem Instead this manual is an attempt to capture and incrementally improve on current best practices in the industry and to give a coherent integrated view of the design process From the Foreword Synopsys and Mentor Graphics have joined forces to help make IP reuse a reality One of the goals of our Design Reuse Partnership is to develop demonstrate and document a reuse based design methodology that works The Reuse Manual RMM is the result of this effort Aart J de Geus Synopsys Inc Walden C Rhines Mentor Graphics Corporation *Hardware and Software: Verification and Testing* Valeria Bertacco,Axel Legay,2013-10-28 This book constitutes the refereed proceedings of the 9th International Haifa Verification Conference HVC 2013 held in Haifa Israel in November 2013 The 24 revised full papers presented were carefully reviewed and selected from 49 submissions The papers are organized in topical sections on SAT and SMT based verification software testing supporting dynamic verification specification and coverage abstraction and model presentation Reuse Methodology Manual for System-on-a-Chip Designs Michael Keating,Pierre Bricaud,2002 Reuse Methodology Manual for System on a Chip Designs Third Edition outlines a set of best practices for creating reusable designs for use in an SoC design methodology These practices are based on the authors experience in developing reusable designs as well as the experience

of design teams in many companies around the world Silicon and tool technologies move so quickly that many of the details of design for reuse will undoubtedly continue to evolve over time But the fundamental aspects of the methodology described in this book have become widely adopted and are likely to form the foundation of chip design for some time to come Development methodology necessarily differs between system designers and processor designers as well as between DSP developers and chipset developers However there is a common set of problems facing everyone who is designing complex chips In response to these problems design teams have adopted a block based design approach that emphasizes design reuse Reusing macros sometimes called cores that have already been designed and verified helps to address all of the problems above However in adopting reuse based design design teams have run into a significant problem Reusing blocks that have not been explicitly designed for reuse has often provided little or no benefit to the team The effort to integrate a pre existing block into new designs can become prohibitively high if the block does not provide the right views the right documentation and the right functionality From this experience design teams have realized that reuse based design requires an explicit methodology for developing reusable macros that are easy to integrate into SoC designs This manual focuses on describing these techniques Features of the Third Edition Up to date State of the art Reuse as a solution for circuit designers A chronicle of best practices All chapters updated and revised Generic guidelines non tool specific Emphasis on hard IP and physical design **An ASIC Low Power Primer** Rakesh Chadha,J. Bhasker,2012-12-05 This book provides an invaluable primer on the techniques utilized in the design of low power digital semiconductor devices Readers will benefit from the hands on approach which starts form the ground up explaining with basic examples what power is how it is measured and how it impacts on the design process of application specific integrated circuits ASICs The authors use both the Unified Power Format UPF and Common Power Format CPF to describe in detail the power intent for an ASIC and then guide readers through a variety of architectural and implementation techniques that will help meet the power intent From analyzing system power consumption to techniques that can be employed in a low power design to a detailed description of two alternate standards for capturing the power directives at various phases of the design this book is filled with information that will give ASIC designers a competitive edge in low power design **Design for Manufacturability and Yield for Nano-Scale CMOS** Charles Chiang,Jamil Kawa,2007-06-15 This book walks the reader through all the aspects of manufacturability and yield in a nano CMOS process It covers all CAD CAE aspects of a SOC design flow and addresses a new topic DFM DFY critical at 90 nm and beyond This book is a must read book the serious practicing IC designer and an excellent primer for any graduate student intent on having a career in IC design or in EDA tool development *Languages, Design Methods, and Tools for Electronic System Design* Daniel Große,Sara Vinco,Hiren Patel,2018-12-19 This book brings together a selection of the best papers from the twentiethedition of the Forum on specification and Design Languages Conference FDL which took place on September 18 20 2017 in Verona Italy FDL is a well established international forum devoted to dissemination of

research results practical experiences and new ideas in the application of specification design and verification languages to the design modeling and verification of integrated circuits complex hardware software embedded systems and mixed technology systems Covers modeling and verification methodologies targeting digital and analog systems Addresses firmware development and validation Targets both functional and non functional properties Includes descriptions of methods for reliable system design **Advanced Verification Topics** Bishnupriya Bhattacharya,John Decker,Gary Hall,Nick Heaton,Yaron Kashai,Neyaz Khan,Zeev Kirshenbaum,Efrat Shneydor,2011-09-30 The Accellera Universal Verification Methodology UVM standard is architected to scale but verification is growing and in more than just the digital design dimension It is growing in the SoC dimension to include low power and mixed signal and the system integration dimension to include multi language support and acceleration These items and others all contribute to the quality of the SOC so the Metric Driven Verification MDV methodology is needed to unify it all into a coherent verification plan This book is for verification engineers and managers familiar with the UVM and the benefits it brings to digital verification but who also need to tackle specialized tasks It is also written for the SoC project manager that is tasked with building an efficient worldwide team While the task continues to become more complex Advanced Verification Topics describes methodologies outside of the Accellera UVM standard but that build on it to provide a way for SoC teams to stay productive and profitable **Winning the SoC Revolution** Grant Martin,Henry Chang,2012-12-06 In 1998 99 at the dawn of the SoC Revolution we wrote Surviving the SOC Revolution A Guide to Platform Based Design In that book we focused on presenting guidelines and best practices to aid engineers beginning to design complex System on Chip devices SoCs Now in 2003 facing the mid point of that revolution we believe that it is time to focus on winning In this book Winning the SoC Revolution Experiences in Real Design we gather the best practical experiences in how to design SoCs from the most advanced design groups while setting the issues and techniques in the context of SoC design methodologies As an edited volume this book has contributions from the leading design houses who are winning in SoCs Altera ARM IBM Philips TI UC Berkeley and Xilinx These chapters present the many facets of SoC design the platform based approach how to best utilize IP Verification FPGA fabrics as an alternative to ASICs and next generation process technology issues We also include observations from Ron Wilson of CMP Media on best practices for SoC design team collaboration We hope that by utilizing this book you too will win the SoC Revolution

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