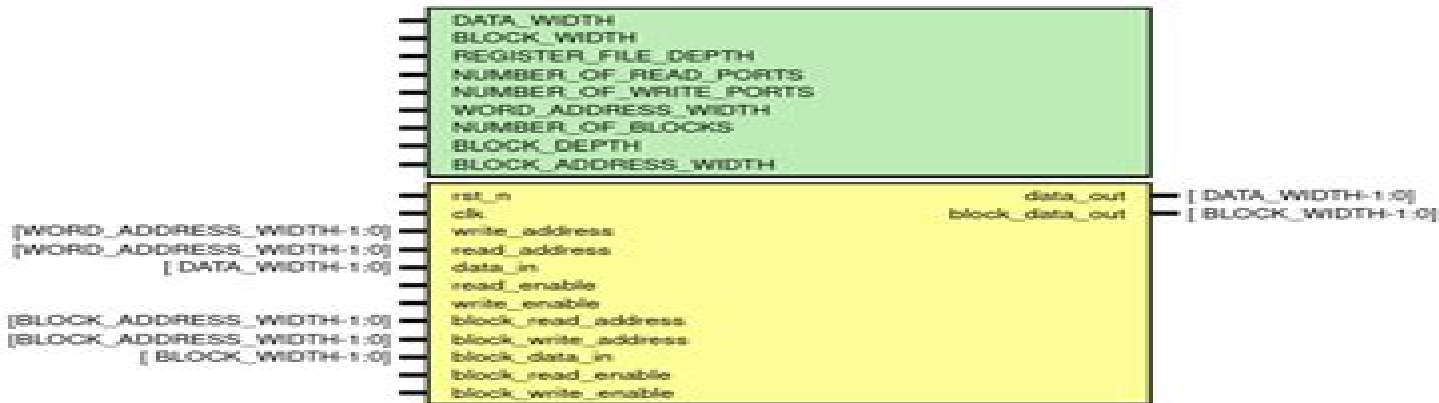


Entity: register_page

• File: register_page.sv

Diagram

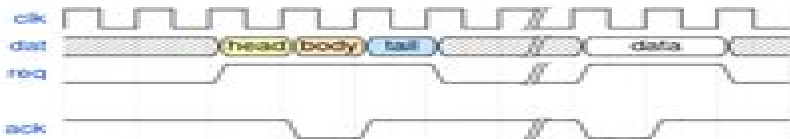


Description

Implements the storage section of the register file

Multiple register_row instances are created according to the parameter.

Timing diagram: This is an example of a read transaction



Generics

Generic name	Type	Value	Description
DATA_WIDTH		16	Width of the data words
BLOCK_WIDTH		256	Width of the blocks, connection between register file and memory
REGISTER_FILE_DEPTH		64	Number of words
NUMBER_OF_READ_PORTS		2	Number of read ports
NUMBER_OF_WRITE_PORTS		1	Number of input ports
WORD_ADDRESS_WIDTH		$\lceil \log_2(\text{REGISTER_FILE_DEPTH}) \rceil$	Length of the address of a word
NUMBER_OF_BLOCKS		BLOCK_WIDTH	Number of blocks accessed by the wide port
BLOCK_DEPTH		BLOCK_WIDTH / DATA_WIDTH	Number of words in a block
BLOCK_ADDRESS_WIDTH		$\lceil \log_2(\text{NUMBER_OF_BLOCKS}) \rceil$	Length of the address of a block

Ports

Port name	Direction	Type	Description
rst_n	input		Asynchronous active low reset
clk	input		Clock signal

Verilog Style Guide

Kathleen Armour



Verilog Style Guide:

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