2. Memory read cycle (3T)

SIGNAL	T,	T ₂	T,
CLOCK			
A ₁₅ -A ₈	HIGHER	ORDER MEMORY	ADDRESS
AD ₇ -AD ₀	LOWER-ORDER MEMORY ADDR	DATA	(D ₇ -D ₉)
ALE			
IO/M,S _{1,} S ₀	\times	10/M = 0, S ₁ = 1	s ₀ = 0
\overline{RD}		-f-V_	

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