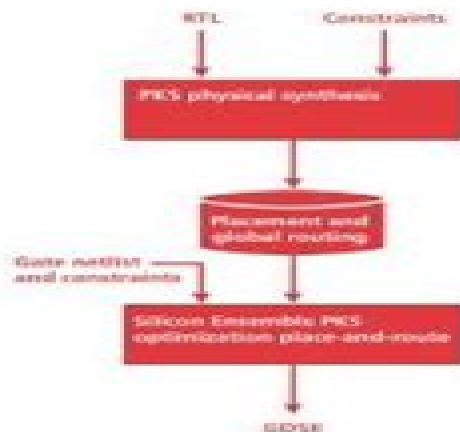


## SILICON ENSEMBLE PKS

Cadence® Silicon Ensemble® Physically Knowledgeable Synthesis (PKS) supports and optimizes an RTL/gates-to-GDSII flow. Production-proven and targeted at 130-nanometer designs and above, Silicon Ensemble PKS is ideal for the design and implementation of mainstream integrated circuits (ICs). However, the Cadence Encounter™ digital IC design platform provides the proven tools and methodologies to implement exceedingly complex, high-performance chips at 130 nanometers and below.



SP&R flow

In addition to its conventional place-and-route features — floorplanning, placement, clock tree synthesis, routing, extraction, and timing analysis — the Silicon Ensemble PKS system also includes PKS concurrent optimization, power analysis, and signal integrity (SI) prevention, analysis, and correction capabilities. These features make the Silicon Ensemble PKS system a solid choice for block-based design and implementation.

### BENEFITS

- Rapid path to tapeout with native timing and design closure features
- Excellent predictability through consistent core technology engines throughout the flow
- Best-in-class SI features enable correct-by-construction design
- Supports 130-nanometer foundry requirements to ease transition to advanced designs

- Multi-CPU routing for enhanced throughput capabilities
- Production-proven with over 15,000 tapeouts worldwide

### COMPLETE RTL-TO-GDSII FLOW

The Silicon Ensemble PKS system is comprised of tightly integrated tools that work in concert to support flows from RTL or gates to GDSII. The RTL-to-GDSII flow begins as PKS synthesizes a physically accurate gate-level netlist. No wireload models are used, and the interconnect delays are based on legal placement and final-quality global routes. A clock tree is also inserted, and post-clock tree optimization is run with the same robust timing engines used consistently throughout the entire flow.

PKS outputs legal placement, clock tree, and global route information to a database that can be forward annotated to the Silicon Ensemble PKS system for final routing. The system reads this

# Silicon Ensemble Manual

**RD Boyd**



## **Silicon Ensemble Manual:**

**From ASICs to SOCs** Farzad Nekoogar, Faranak Nekoogar, 2003 From ASICs to SOCs A Practical Approach by Farzad Nekoogar and Faranak Nekoogar covers the techniques principles and everyday realities of designing ASICs and SOCs Material includes current issues in the field front end and back end designs integration of IPs on SOC designs and low power design techniques and methodologies Appropriate for practicing chip designers as well as graduate students in electrical engineering

**Reuse Techniques for VLSI Design** Ralf Seepold, Arno Kunzmann, 2012-12-06 Reuse Techniques for VLSI Design is a reflection on the current state of the art in design reuse for microelectronic systems To that end it is the first book to garner the input of leading experts from both research and application areas These experts document herein not only their more mature approaches but also their latest research results Firstly it sets out the background and support from international organisations that enforce System on a Chip SoC design by reuse oriented methodologies This overview is followed by a number of technical presentations covering different requirements of the reuse domain These are presented from different points of view i e IP provider IP user designer isolated reuse intra company or inter company reuse More general systems or case studies e g metrics are followed by comprehensive reuse systems e g reuse management systems partly including business models Since design reuse must not be restricted to digital components mixed signal and analog reuse approaches are also presented In parallel to the digital domain this area covers research in reuse database design Design verification and legal aspects are two important topics that are closely related to the realization of design reuse These hot topics are covered by presentations that finalize the survey of outstanding research development and application of design reuse for SoC design Reuse Techniques for VLSI Design is an invaluable reference for researchers and engineers involved in VLSI ASIC design

**Analysis and Design of Resilient VLSI Circuits** Rajesh Garg, 2009-10-22 This monograph is motivated by the challenges faced in designing reliable VLSI systems in modern VLSI processes The reliable operation of integrated circuits ICs has become increasingly difficult to achieve in the deep submicron DSM era With continuously decreasing device feature sizes combined with lower supply voltages and higher operating frequencies the noise immunity of VLSI circuits is decreasing alarmingly Thus VLSI circuits are becoming more vulnerable to noise effects such as crosstalk power supply variations and radiation induced soft errors Among these noise sources soft errors or error caused by radiation particle strikes have become an increasingly troublesome issue for memory arrays as well as combinational logic circuits Also in the DSM era process variations are increasing at a significant rate making it more difficult to design reliable VLSI circuits Hence it is important to efficiently design robust VLSI circuits that are resilient to radiation particle strikes and process variations The work presented in this research monograph presents several analysis and design techniques with the goal of realizing VLSI circuits which are radiation and process variation tolerant

Physical Diagnosis Tool to Locate and Analyze Logical Faults on a Chip Archana Gupta, 2005

**The VLSI Handbook** Wai-Kai Chen, 2019-07-17 Over the years the

fundamentals of VLSI technology have evolved to include a wide range of topics and a broad range of practices To encompass such a vast amount of knowledge The VLSI Handbook focuses on the key concepts models and equations that enable the electrical engineer to analyze design and predict the behavior of very large scale integrated circuits It provides the most up to date information on IC technology you can find Using frequent examples the Handbook stresses the fundamental theory behind professional applications Focusing not only on the traditional design methods it contains all relevant sources of information and tools to assist you in performing your job This includes software databases standards seminars conferences and more The VLSI Handbook answers all your needs in one comprehensive volume at a level that will enlighten and refresh the knowledge of experienced engineers and educate the novice This one source reference keeps you current on new techniques and procedures and serves as a review for standard practice It will be your first choice when looking for a solution

*Proceedings*, 1998      Microelectronics Education Adrian M. Ionescu, Michel Declercq, Maher Kayal, Yusuf Leblebici, 2013-03-19 In this book key contributions on developments and challenges in research and education on microelectronics microsystems and related areas are published Topics of interest include but are not limited to emerging fields in design and technology new concepts in teaching multimedia in microelectronics industrial roadmaps and microelectronic education curricula nanoelectronics teaching long distance education The book is intended for academic education level and targets professors researchers and PhDs involved in microelectronics and or more generally in electrical engineering microsystems and material sciences The 2004 edition of European Workshop on Microelectronics Education EWME is particularly focused on the interface between microelectronics and bio medical sciences      Custom-cell Based Domain-specific Macro Generation for Digital Signal Processing Applications Joyopriya Bakshi, 2004      **Official Gazette of the United States Patent and Trademark Office**, 1996      **CERN**. Institut de recherches subatomiques de Strasbourg, 2002      Manuals Combined: 30+ Army Navy And Air Force Aviation EJECTION SEAT Studies, Just a SAMPLE of the CONTENTS 1 Full Text pdf 5 MB Title Steam Vapor Cleaning Ejection Seat Frames and Components Technical Evaluation AD Number ADA412405 Corporate Author NAVAL AIR WARFARE CENTER AIRCRAFT DIV PATUXENT RIVER MD Personal Author Kwan R M Yost A J Santiago J V Herring A C Conlin M M Report Date March 19 2003 Media 86 Pages s Distribution Code 01 APPROVED FOR PUBLIC RELEASE Report Classification Not Available Source Code 424295 From the collection Technical 2 Full Text pdf 5 MB Title Using the GPS to Improve Trajectory Position and Velocity Determination During Real Time Ejection Seat Test and Evaluation AD Number ADA415240 Corporate Author AIR FORCE INST OF TECH WRIGHT PATTERSON AFB OH SCHOOL OF ENGINEERING AND MANAGEMENT Personal Author Schutte Christina G Report Date February 01 2003 Media 127 Pages s Distribution Code 01 APPROVED FOR PUBLIC RELEASE 26 NOT AVAILABLE IN MICROFICHE Report Classification Not Available Source Code 439106 From the collection Technical 3 Full Text pdf 4 MB Title Using the GPS to Collect Trajectory Data for Ejection Seat Design Validation and Testing AD Number

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**Cross-Talk Noise Immune VLSI Design Using Regular Layout Fabrics** Robert K. Brayton,Alberto L. Sangiovanni-Vincentelli,2012-12-06 This book was motivated by the problems being faced with shrinking IC process feature sizes It is well known that as process feature sizes shrink a host of electrical problems like cross talk electromigration self heat etc are becoming important Cross talk is one of the major problems since it results in unpredictable design behavior In particular it can result in significant delay variation or signal integrity problems in a wire depending on the state of its neighboring wires Typical approaches to tackle the cross talk problem attempt to fix the problem once it is created In our approach we ensure that cross talk is eliminated by design The work described in this book attempts to take an outside the box view and propose a radically different design style This design style first imposes a fixed layout pattern or fabric on the integrated circuit and then embeds the circuit being implemented into this fabric The fabric is chosen carefully in order to eliminate the cross talk problem being faced in modem IC processes With our choice of fabric cross talk between adjacent wires on an IC is reduced by between one and two orders of magnitude In this way the fabric concept eliminates cross talk up front and by design We propose two separate design flows each of which uses the fabric concept to implement logic The first flow uses fabric compliant standard cells as an implementation vehicle We call these cells fabric cells and they have the same logic functionality as existing standard cells with which they are compared

Digital Synthesizers and Transmitters for Software Radio Jouko Vankka,2005-07-22 The approach adopted in Digital Synthesizers and Transmitters for Software Radio will provide an understanding of key areas in the field of digital synthesizers and transmitters It is easy to include different digital techniques in the digital synthesizers and transmitters by using digital signal processing methods because the signal is in digital form By programming the digital synthesizers and transmitters adaptive channel bandwidths modulation formats frequency hopping and data rates are easily achieved Techniques such as digital predistortion for power amplifier linearization digital compensation methods for analog I Q modulator nonlinearities and digital power control and ramping are presented in this book The flexibility of the digital synthesizers and transmitters makes them ideal as signal generators for software radio Software radios represent a major change in the design paradigm for radios in which a large portion of the functionality is implemented through programmable signal processing devices giving the radio the ability to change its operating parameters to accommodate new features and



capabilities A software radio approach reduces the content of radio frequency RF and other analog components of traditional radios and emphasizes digital signal processing to enhance overall transmitter flexibility Software radios are emerging in commercial and military infrastructure Minimizing and Exploiting Leakage in VLSI Design Nikhil Jayakumar, Suganth Paul, Rajesh Garg, 2009-12-02 Power consumption of VLSI Very Large Scale Integrated circuits has been growing at an alarmingly rapid rate This increase in power consumption coupled with the increasing demand for portable hand held electronics has made power consumption a dominant concern in the design of VLSI circuits today Traditionally dynamic switching power has dominated the total power consumption of an IC However due to current scaling trends leakage power has now become a major component of the total power consumption in VLSI circuits Leakage power reduction is especially important in portable hand held electronics such as cell phones and PDAs This book presents two techniques aimed at reducing leakage power in digital VLSI ICs The first technique reduces leakage through the selective use of high threshold voltage sleep transistors The second technique reduces leakage by applying the optimal Reverse Body Bias RBB voltage This book also shows readers how to turn the leakage problem into an opportunity through the use of sub threshold logic

Official Gazette of the United States Patent and Trademark Office ,1996 **Interconnect Noise Optimization in Nanometer Technologies** Mohamed Elgamel, Magdy A. Bayoumi, 2006-03-20 Interconnect has become the dominating factor in determining system performance in nanometer technologies Dedicated to this subject Interconnect Noise Optimization in Nanometer Technologies provides insight and intuition into layout analysis and optimization for interconnect in high speed high complexity integrated circuits The authors bring together a wealth of information presenting a range of CAD algorithms and techniques for synthesizing and optimizing interconnect Practical aspects of the algorithms and the models are explained with sufficient details The book investigates the most effective parameters in layout optimization Different post layout optimization techniques with complexity analysis and benchmarks tests are provided The impact crosstalk noise and coupling on the wire delay is analyzed Parameters that affect signal integrity are also considered

**International Conference on Simulation of Semiconductor Processes and Devices** ,2003 **IEEE, ACM International Conference on Computer Aided Design** International Conference on Computer Aided Design. Institute of Electrical and Electronics Engineers, 2000, San José, Calif., 2000 **Smart Power Integration** Mohamed Abouelatta, Ahmed Shaker, Christian Gontrand, 2022-10-18 Smart power integration is at the crossroads of different fields of electronics such as high and low power engine control and electrothermal studies of devices and circuits These circuits are complex and are heavily influenced by substrate coupling especially where 3D integration is concerned This book provides an overview of smart power integration including high voltage devices dedicated and compatible processes as well as isolation techniques Two types of integration are highlighted modular or hybrid integration together with compatible devices such as the insulated gate bipolar transistor IGBT and monolithic integration specifically through the paradigm of functional

integration Smart Power Integration outlines the main MOS devices for high voltage integrated circuits and explores into the fields of codesign coupling hardware and software design including applications to motor control Studies focusing on heat pipes for electronics cooling are also outlined      **Electronics Computer Aided Design** Phil L. Jones, Anne Buckley, 1989

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