

VERILOG PROJECT

VEDIC MULTIPLIER ✕



8-Bit Multiplier

```
module veda_8bitmultiplier
input [7:0]a;
input [7:0]b;
output [15:0]c;

wire [15:0]p0;
wire [15:0]p1;
wire [15:0]p2;
wire [15:0]p3;
wire [15:0]p4;
wire [15:0]p5;
wire [15:0]p6;
wire [15:0]p7;
wire [15:0]p8;
wire [15:0]p9;
wire [15:0]p10;
wire [15:0]p11;
wire [15:0]p12;
wire [15:0]p13;
wire [15:0]p14;
wire [15:0]p15;

p0: a[0] & b[0] ? a[0] & b[0] : 0;
p1: a[0] & b[1] ? a[0] & b[1] : 0;
p2: a[0] & b[2] ? a[0] & b[2] : 0;
p3: a[0] & b[3] ? a[0] & b[3] : 0;
p4: a[0] & b[4] ? a[0] & b[4] : 0;
p5: a[0] & b[5] ? a[0] & b[5] : 0;
p6: a[0] & b[6] ? a[0] & b[6] : 0;
p7: a[0] & b[7] ? a[0] & b[7] : 0;
p8: a[1] & b[0] ? a[1] & b[0] : 0;
p9: a[1] & b[1] ? a[1] & b[1] : 0;
p10: a[1] & b[2] ? a[1] & b[2] : 0;
p11: a[1] & b[3] ? a[1] & b[3] : 0;
p12: a[1] & b[4] ? a[1] & b[4] : 0;
p13: a[1] & b[5] ? a[1] & b[5] : 0;
p14: a[1] & b[6] ? a[1] & b[6] : 0;
p15: a[1] & b[7] ? a[1] & b[7] : 0;

assign c[0] = p0;
assign c[1] = p0 & 1;
assign c[2] = p0 & 2;
assign c[3] = p0 & 4;
assign c[4] = p0 & 8;
assign c[5] = p0 & 16;
assign c[6] = p0 & 32;
assign c[7] = p0 & 64;
assign c[8] = p1;
assign c[9] = p1 & 1;
assign c[10] = p1 & 2;
assign c[11] = p1 & 4;
assign c[12] = p1 & 8;
assign c[13] = p1 & 16;
assign c[14] = p1 & 32;
assign c[15] = p1 & 64;

endmodule
```

(Code for 8 bit multiplier)

4-Bit Multiplier

```
module veda_4bitmultiplier
input [3:0]a;
input [3:0]b;
output [7:0]c;

wire [7:0]p0;
wire [7:0]p1;
wire [7:0]p2;
wire [7:0]p3;
wire [7:0]p4;
wire [7:0]p5;
wire [7:0]p6;
wire [7:0]p7;
wire [7:0]p8;
wire [7:0]p9;
wire [7:0]p10;
wire [7:0]p11;
wire [7:0]p12;
wire [7:0]p13;
wire [7:0]p14;
wire [7:0]p15;

p0: a[0] & b[0] ? a[0] & b[0] : 0;
p1: a[0] & b[1] ? a[0] & b[1] : 0;
p2: a[0] & b[2] ? a[0] & b[2] : 0;
p3: a[0] & b[3] ? a[0] & b[3] : 0;
p4: a[1] & b[0] ? a[1] & b[0] : 0;
p5: a[1] & b[1] ? a[1] & b[1] : 0;
p6: a[1] & b[2] ? a[1] & b[2] : 0;
p7: a[1] & b[3] ? a[1] & b[3] : 0;
p8: a[2] & b[0] ? a[2] & b[0] : 0;
p9: a[2] & b[1] ? a[2] & b[1] : 0;
p10: a[2] & b[2] ? a[2] & b[2] : 0;
p11: a[2] & b[3] ? a[2] & b[3] : 0;
p12: a[3] & b[0] ? a[3] & b[0] : 0;
p13: a[3] & b[1] ? a[3] & b[1] : 0;
p14: a[3] & b[2] ? a[3] & b[2] : 0;
p15: a[3] & b[3] ? a[3] & b[3] : 0;

assign c[0] = p0;
assign c[1] = p0 & 1;
assign c[2] = p0 & 2;
assign c[3] = p0 & 4;
assign c[4] = p0 & 8;
assign c[5] = p0 & 16;
assign c[6] = p0 & 32;
assign c[7] = p0 & 64;

endmodule
```

(Code for 4 bit multiplier)

```
0 = 00000000, 0=00000000, --- = 0000000000000000
100 = 00000000, 0=00000000, --- = 0000000000000000
100 = 00000000, 0=00000000, --- = 0000000000000000
100 = 00000000, 0=00000000, --- = 0000000000000000
100 = 00000000, 0=00000000, --- = 0000000000000000
100 = 00000000, 0=00000000, --- = 0000000000000000
```

(c gives the multiplication of a and b)



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**Pradeep Kumar Mallick, Valentina
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Advances in Multidisciplinary Medical Technologies – Engineering, Modeling and Findings Abdeldjalil

Khelassi, Vania Vieira Estrela, 2020-11-07 This book collects the proceedings of the International Congress on Health Sciences and Medical Technologies ICHSMT held in Tlemcen, Algeria, from December 5 to 7, 2019. The proceedings present a forum for the latest projects and research in scientific and technological development with an emphasis on smart healthcare system design and future technologies. ICHSMT brings together researchers, students, and professionals from the healthcare, corporate, and academic sectors. It includes a far-reaching program supported by a variety of technical tracks that seek to promote medical technologies and innovation at a nationwide level. **Advances in Electrical and Computer**

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