

VERILOG PROJECT

× × N-Bit Multiplier with × ×
× × Binary to BCD × ×
× × Conversion × ×
× × × ×

```
// Continuous assignment
always bus = bus_reg;
always out = out_reg;
always finish = finish_reg;

integer i;
```

Continuous Assignments

```
// Reset clk and inputs
always @posedge reset;
begin
    out_reg = 0;
    a_in_reg = 0;
    b_in_reg = 0;
end
```

Reset clk and inputs

```
always @posedge clk;
begin
    if (reset)
        begin
```

```
            // Reset outputs
            out_reg = 0;
            a_in_reg = a_in;
            b_in_reg = b_in;
            out = 0;
            finish_reg = 0;
            out_reg = 0;
            bus_reg = 0;
            $display("Data loaded into the input registers");
        end
```

```
always @posedge clk;
    process(a_in, b_in)
    begin
```

```
        // Inputs
        reg [31:0] prod = 0;
        reg [31:0] a_in;
        reg [31:0] b_in;
        reg out;
        reg finish;
```

```
        // Outputs
        wire [31:0] prod_reg;
        wire finish_reg;
        wire [31:0] bus_reg;
        wire [31:0] out_reg;
        wire [31:0] finish_reg;
```

```
        // Multiplication and BCD conversion
```

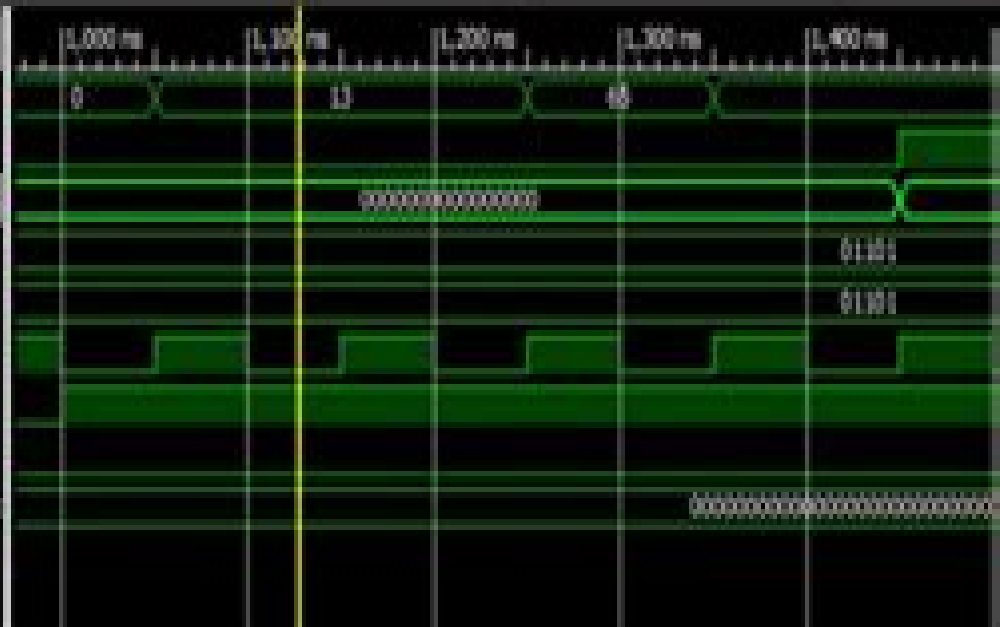
```
        multiplicate with i
        begin
            a_in = a_in;
            b_in = b_in;
            out = 0;
            finish = 0;
            finish_reg = 0;
            out_reg = 0;
            bus_reg = 0;
        end
```

```
        // Delayed output
        out_reg = out;
```

```
        // Delayed output
        finish_reg = finish;
        bus_reg = bus;
    end
```



Name	Value
out[3:0]	13
finish	0
bus[31:0]	0000000000000000
a_in[4:0]	01101
b_in[4:0]	01101
clk	0
start	1
reset	0
a_in[31:0]	0000000000000000



Verilog Code For Multiplier

Uwe Meyer-Baese

A red circular graphic with a gradient, appearing as a semi-circle or a partial circle, located to the right of the author's name.

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