

VERILOG PROJECT

VEDIC MULTIPLIER ✕



8-Bit Multiplier

```
module veda_8bitmultiplier
input [7:0]a;
input [7:0]b;
output [15:0]c;

wire [15:0]p0;
wire [15:0]p1;
wire [15:0]p2;
wire [15:0]p3;
wire [15:0]p4;
wire [15:0]p5;
wire [15:0]p6;
wire [15:0]p7;
wire [15:0]p8;
wire [15:0]p9;
wire [15:0]p10;
wire [15:0]p11;
wire [15:0]p12;
wire [15:0]p13;
wire [15:0]p14;
wire [15:0]p15;

p0: a[0] & b[0] <= p0[0] & b[0];
p1: a[0] & b[1] <= p1[0] & b[1];
p2: a[0] & b[2] <= p2[0] & b[2];
p3: a[0] & b[3] <= p3[0] & b[3];
p4: a[0] & b[4] <= p4[0] & b[4];
p5: a[0] & b[5] <= p5[0] & b[5];
p6: a[0] & b[6] <= p6[0] & b[6];
p7: a[0] & b[7] <= p7[0] & b[7];
p8: a[1] & b[0] <= p8[0] & b[0];
p9: a[1] & b[1] <= p9[0] & b[1];
p10: a[1] & b[2] <= p10[0] & b[2];
p11: a[1] & b[3] <= p11[0] & b[3];
p12: a[1] & b[4] <= p12[0] & b[4];
p13: a[1] & b[5] <= p13[0] & b[5];
p14: a[1] & b[6] <= p14[0] & b[6];
p15: a[1] & b[7] <= p15[0] & b[7];

c[0] = p0[0];
c[1] = p0[1] + p1[0];
c[2] = p0[2] + p1[1] + p2[0];
c[3] = p0[3] + p1[2] + p2[1] + p3[0];
c[4] = p0[4] + p1[3] + p2[2] + p3[1] + p4[0];
c[5] = p0[5] + p1[4] + p2[3] + p3[2] + p4[1] + p5[0];
c[6] = p0[6] + p1[5] + p2[4] + p3[3] + p4[2] + p5[1] + p6[0];
c[7] = p0[7] + p1[6] + p2[5] + p3[4] + p4[3] + p5[2] + p6[1] + p7[0];
c[8] = p1[7] + p2[6] + p3[5] + p4[4] + p5[3] + p6[2] + p7[1] + p8[0];
c[9] = p1[8] + p2[7] + p3[6] + p4[5] + p5[4] + p6[3] + p7[2] + p8[1] + p9[0];
c[10] = p1[9] + p2[8] + p3[7] + p4[6] + p5[5] + p6[4] + p7[3] + p8[2] + p9[1] + p10[0];
c[11] = p1[10] + p2[9] + p3[8] + p4[7] + p5[6] + p6[5] + p7[4] + p8[3] + p9[2] + p10[1] + p11[0];
c[12] = p1[11] + p2[10] + p3[9] + p4[8] + p5[7] + p6[6] + p7[5] + p8[4] + p9[3] + p10[2] + p11[1] + p12[0];
c[13] = p1[12] + p2[11] + p3[10] + p4[9] + p5[8] + p6[7] + p7[6] + p8[5] + p9[4] + p10[3] + p11[2] + p12[1] + p13[0];
c[14] = p1[13] + p2[12] + p3[11] + p4[10] + p5[9] + p6[8] + p7[7] + p8[6] + p9[5] + p10[4] + p11[3] + p12[2] + p13[1] + p14[0];
c[15] = p1[14] + p2[13] + p3[12] + p4[11] + p5[10] + p6[9] + p7[8] + p8[7] + p9[6] + p10[5] + p11[4] + p12[3] + p13[2] + p14[1] + p15[0];
endmodule
```

(Code for 8 bit multiplier)

4-Bit Multiplier

```
module veda_4bitmultiplier
input [3:0]a;
input [3:0]b;
output [7:0]c;

wire [7:0]p0;
wire [7:0]p1;
wire [7:0]p2;
wire [7:0]p3;
wire [7:0]p4;
wire [7:0]p5;
wire [7:0]p6;
wire [7:0]p7;
wire [7:0]p8;
wire [7:0]p9;
wire [7:0]p10;
wire [7:0]p11;
wire [7:0]p12;
wire [7:0]p13;
wire [7:0]p14;
wire [7:0]p15;

p0: a[0] & b[0] <= p0[0] & b[0];
p1: a[0] & b[1] <= p1[0] & b[1];
p2: a[0] & b[2] <= p2[0] & b[2];
p3: a[0] & b[3] <= p3[0] & b[3];
p4: a[1] & b[0] <= p4[0] & b[0];
p5: a[1] & b[1] <= p5[0] & b[1];
p6: a[1] & b[2] <= p6[0] & b[2];
p7: a[1] & b[3] <= p7[0] & b[3];
p8: a[2] & b[0] <= p8[0] & b[0];
p9: a[2] & b[1] <= p9[0] & b[1];
p10: a[2] & b[2] <= p10[0] & b[2];
p11: a[2] & b[3] <= p11[0] & b[3];
p12: a[3] & b[0] <= p12[0] & b[0];
p13: a[3] & b[1] <= p13[0] & b[1];
p14: a[3] & b[2] <= p14[0] & b[2];
p15: a[3] & b[3] <= p15[0] & b[3];

c[0] = p0[0];
c[1] = p0[1] + p1[0];
c[2] = p0[2] + p1[1] + p2[0];
c[3] = p0[3] + p1[2] + p2[1] + p3[0];
c[4] = p1[3] + p2[2] + p3[1] + p4[0];
c[5] = p1[4] + p2[3] + p3[2] + p4[1] + p5[0];
c[6] = p1[5] + p2[4] + p3[3] + p4[2] + p5[1] + p6[0];
c[7] = p1[6] + p2[5] + p3[4] + p4[3] + p5[2] + p6[1] + p7[0];
c[8] = p2[6] + p3[5] + p4[4] + p5[3] + p6[2] + p7[1] + p8[0];
c[9] = p2[7] + p3[6] + p4[5] + p5[4] + p6[3] + p7[2] + p8[1] + p9[0];
c[10] = p2[8] + p3[7] + p4[6] + p5[5] + p6[4] + p7[3] + p8[2] + p9[1] + p10[0];
c[11] = p2[9] + p3[8] + p4[7] + p5[6] + p6[5] + p7[4] + p8[3] + p9[2] + p10[1] + p11[0];
c[12] = p2[10] + p3[9] + p4[8] + p5[7] + p6[6] + p7[5] + p8[4] + p9[3] + p10[2] + p11[1] + p12[0];
c[13] = p2[11] + p3[10] + p4[9] + p5[8] + p6[7] + p7[6] + p8[5] + p9[4] + p10[3] + p11[2] + p12[1] + p13[0];
c[14] = p2[12] + p3[11] + p4[10] + p5[9] + p6[8] + p7[7] + p8[6] + p9[5] + p10[4] + p11[3] + p12[2] + p13[1] + p14[0];
c[15] = p2[13] + p3[12] + p4[11] + p5[10] + p6[9] + p7[8] + p8[7] + p9[6] + p10[5] + p11[4] + p12[3] + p13[2] + p14[1] + p15[0];
endmodule
```

(Code for 4 bit multiplier)

```
0 = 00000000, 0=00000000, --- = 0000000000000000
100 = 00000100, 0=00000000, --- = 0000000000000000
100 = 00000100, 0=00000000, --- = 0000000000000000
100 = 00000100, 0=00000000, --- = 0000000000000000
100 = 00000100, 0=00000000, --- = 0000000000000000
100 = 00000100, 0=00000000, --- = 0000000000000000
100 = 00000100, 0=00000000, --- = 0000000000000000
```

(c gives the multiplication of a and b)



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**Veena S. Chakravarthi, Yasha Jyothi M.
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