16

III B.Tech II Semester Regular Examinations, Apr/May 2008 VLSI DESIGN

(Common to Electronics & Communication Engineering, Bio-Medical Engineering and Electronics & Telematics)

Time: 3 hours

nswer any FIVE Questions Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks

- 1. Describe the two commonly used methods for obtaining integrated capacitor.
- (a) Explain various regions of CMOS inverter transfer characteristics.
 - (b) For a CMOS inverter, calculate the shift in the transfer characteristic curve when β_n/β_p ratio is varied from 1/1 to 10/1. [8+8]
- (a) what is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.
 - (b) What are the effects of scaling on V_I?
 - (c) What are design rules? Why is metal- metal spacing larger than poly -poly spacing. [8+4+4]
- Calculate the rise time and fall time of the CMOS inverter (W/L)_n= 6 and (W/L)_p=8, K'_n =150μ A/V², V_{tn} =0.7V,K'_p= 62 μ A/V², V_{tp}=-0.85V , V_{DD} =3.3V. Total output capacitance =150 fF. [16]
- (a) Explain the CMOS system design based on the data path operators with a suitable example.
 - (b) Draw and explain the basic Memory- chip architecture. [8+8]
- (a) Draw the typical standard-cell structure showing low-power cell and explain it.
 - (b) Sketch a diagram for two input XOR using PLA and explain its operation with the help of truth table. [8+8]
- (a) Write a VHDL Program for a divide-by-3 counter with suitable state diagram.
 - (b) Compare all available design verification tools. [8+8]
- (a) Explain how an improved layout can be reduced faults in CMOS circuits.
 - (b) Explain how a pseudo random sequence generator may be used to test a 16-bit data path. How would the outputs be collected and checked. [6+10]

ALC: NO DECIMAL DECIMA

Vlsi Cmos Design Question Paper

Tao Wei

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