

UNIT I: INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS

9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II: RETIMING, ALGORITHMIC STRENGTH REDUCTION

9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III: FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS

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Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV: SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES

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Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V: NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING

9

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining, Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL: 45 PERIODS

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1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation", Wiley, Interscience, 2007.
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.

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VLSI Signal Processing, VI IEEE Acoustics, Speech, and Signal Processing Society, 1993 *VLSI Analog Signal Processing Circuits* Hongjiang Song, 2014-02-14 This book is based on a collection of the past exams for the VLSI Analog Signal Processing Circuits class EEE598 the author offered in the School of Engineering at Arizona State University The topics cover various aspects of the design analysis and application of VLSI analog signal processing circuits This book is intended to be used together with the VLSI Analog Signal Processing Circuits textbook by the same author It can also be used alone for the experienced readers *VLSI Signal Processing Architectures* Institution of Electrical Engineers. Electronics Division. Professional Groups E10 (Circuit Theory and Design), E4 (Image Processing and Vision) and E5 (Signal Processing), 1990 Digital Signal Processing for VLSI Institution of Electrical Engineers. Electronics Division. Professional Group E10 (Circuit Theory and Design), 1988 VLSI Signal Processing Systems Earl E. Swartzlander, 1986 VLSI and Modern Signal Processing , VLSI Digital Signal Processing Systems Keshab K. Parhi, 1999 *High-performance VLSI Signal Processing* K. J. Ray Liu, Kung Yao, 1998 Advances in VLSI, Communication, and Signal Processing David Harvey, Haranath Kar, Shekhar Verma, Vijaya Bhadauria, 2020-10-14 This book comprises select peer reviewed papers from the International Conference on VLSI Communication and Signal processing VCAS 2019 held at Motilal Nehru National Institute of Technology MNNIT Allahabad Prayagraj India The contents focus on latest research in different domains of electronics and communication engineering in particular microelectronics and VLSI design communication systems and networks and signal and image processing The book also discusses the emerging applications of novel tools and techniques in image video and multimedia signal processing This book will be useful to students researchers and professionals working in the electronics and communication domain *VLSI Signal Processing Technology* Magdy Bayoumi, Earl Swartzlander, 1994-10-31 This book is the first in a set of forthcoming books focussed on state of the art development in the VLSI Signal Processing area It is a response to the tremendous research activities taking place in that field These activities have been driven by two factors the dramatic increase in demand for high speed signal processing especially in consumer electronics and the evolving microelectronic technologies The available technology has always been one of the main factors in determining algorithms architectures and design strategies to be followed With every new technology signal processing systems go through many changes in concepts design methods and implementation The goal of this book is to introduce the reader to the main features of VLSI Signal Processing and the ongoing developments in this area The focus of this book is on Current developments in Digital Signal Processing DSP processors and architectures several examples and case studies of existing DSP chips are discussed in Chapter 1 Features and requirements of image and video signal processing architectures both applications specific integrated circuits ASICs and programmable image processors are studied in Chapter 2 New market areas for signal processing especially in consumer electronics such as multimedia teleconferencing and movie on

demand Impact of arithmetic circuitry on the performance of DSP pro cessors several topics are discussed in Chapter 3 such
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