

Simulating Verilog RTL using Synopsys VCS

6.375 Tutorial 1
February 1, 2008

In this tutorial you will gain experience using Synopsys VCS to compile cycle-accurate executable simulators from Verilog RTL. You will also learn how to use the Synopsys Waveform viewer to trace the various signals in your design. Figure 1 illustrates the basic VCS and SMIPS assembler toolflow. VCS takes a set of Verilog files as input and produces a simulator. When we execute the simulator we need some way to observe our design so that we can measure its performance and verify that it is working correctly. There are two primary ways to observe our design: (1) we can use `$display` statements in our Verilog RTL to output textual trace information, or (2) we can instruct the simulator to automatically write transition information about each signal in our design to a file. There is standard text format for this type of signal transition trace information called the Value Change Dump format (VCD). Unfortunately, these textual trace files can become very large very quickly, so Synopsys uses a proprietary compressed binary trace format called VCD Plus (VPD). We can view VPD files using the Synopsys waveform viewer called VirSim.

We will be using a simple unpipelined SMIPSV1 processor as our design example for this tutorial, and thus you will also learn the how to build and run test codes on the processor simulator. Figure 2 shows the block diagram for the example processor. Figure 1 shows the SMIPS assembler toolflow which starts with an SMIPS assembly file and uses several tools to generate a Verilog Memory Hex (VMH) file suitable to run on the cycle-accurate simulator. This tutorial assumes you are familiar with the SMIPS ISA. For more information please consult the *SMIPS Processor Specification*.

For more information consult the CVS user manual ([cvs-user-guide.pdf](#)) located in the course locker ([/mit/6.375/doc](#)).

Getting started

Before using the 6.375 toolflow you must add the course locker and run the course setup script with the following two commands.

```
% add 6.375
% source /mit/6.375/setup.csh
```

Vcs Getting Started Guide

F Rizvi



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GitLab Quick Start Guide Adam O'Grady,2018-11-30 Port projects

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The Scalyr Guide to Getting Started Logging as Quickly as Possible Scalyr, 2019-04-07 With the almost constant scaling of applications and environments the need for good logging practices has likewise scaled exponentially This book will help you understand the value of logging the best practices for logs and introduce you to a number of tech stacks including languages and frameworks It s the ultimate resource for jumping into a new language or discovering new tricks in a familiar one And you ll learn the value that centralized logging brings on scale All proceeds from this book will be donated by Scalyr to Girls Who Code

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Vectorworks for Entertainment Design Kevin Lee Allen, 2020-05-26 Vectorworks for Entertainment Design covers the complete design process for using Vectorworks in entertainment industry from developing ideas visualizing ideas and evolving them for execution This second edition has been extensively revised and updated covering the most current details of the Vectorworks software for scenery lighting sound and rigging real and virtually With a focused look at the production process from ideation to development to

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The Business of Venture Capital Mahendra Ramsinghani, 2021-02-03 The new edition of the

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