

VERILOG PROJECT

VEDIC MULTIPLIER ✕



8-Bit Multiplier

```
module veda_8bits_8x8 {
    input [7:0]a;
    input [7:0]b;
    output [15:0]c;

    wire [15:0]p0;
    wire [15:0]p1;
    wire [15:0]p2;
    wire [15:0]p3;
    wire [15:0]p4;
    wire [15:0]p5;
    wire [15:0]p6;
    wire [15:0]p7;
    wire [15:0]p8;
    wire [15:0]p9;
    wire [15:0]p10;
    wire [15:0]p11;
    wire [15:0]p12;
    wire [15:0]p13;
    wire [15:0]p14;
    wire [15:0]p15;

    veda_8x8_0 a,b,p0,p1,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;
    veda_8x8_1 a,b,p1,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;
    veda_8x8_2 a,b,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;
    veda_8x8_3 a,b,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;

    assign temp0 = (a[7]&b[7])<16;
    add_8_bits temp0[15:0],temp0[15:0];
    assign temp1 = (a[7]&b[6])<15;
    assign temp2 = (a[7]&b[5])<14;
    assign temp3 = (a[7]&b[4])<13;
    add_16_bits temp0,temp1,temp2,temp3;
    assign temp4 = (a[7]&b[3])<12;
    add_16_bits temp4,temp4,temp4,temp4;

    add_16_bits temp4,temp4,temp4,temp4;

    assign c[15:0] = temp4;
    assign c[15:0] = temp4;
endmodule
```

(Code for 8 bit multiplier)

4-Bit Multiplier

```
module veda_4x4_4bits_4x4 {
    input [3:0]a;
    input [3:0]b;
    output [7:0]c;

    wire [7:0]p0;
    wire [7:0]p1;
    wire [7:0]p2;
    wire [7:0]p3;
    wire [7:0]p4;
    wire [7:0]p5;
    wire [7:0]p6;
    wire [7:0]p7;
    wire [7:0]p8;
    wire [7:0]p9;
    wire [7:0]p10;
    wire [7:0]p11;
    wire [7:0]p12;
    wire [7:0]p13;
    wire [7:0]p14;
    wire [7:0]p15;

    veda_4x4_0 a,b,p0,p1,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;
    veda_4x4_1 a,b,p1,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;
    veda_4x4_2 a,b,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;
    veda_4x4_3 a,b,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,p14,p15;

    assign temp1 = (a[3]&b[3])<8;
    add_4_bits temp1[7:0],temp1[7:0];
    assign temp2 = (a[3]&b[2])<7;
    assign temp3 = (a[3]&b[1])<6;
    add_4_bits temp1,temp2,temp3,temp3;

    assign temp4 = (a[3]&b[0])<5;
    add_4_bits temp4,temp4,temp4,temp4;
    assign c[7:0] = temp4;
endmodule
```

(Code for 4 bit multiplier)

```
0 = 00000000, 0=00000000, --- = 0000000000000000
100 = 00000000, 0=00000000, --- = 0000000000000000
100 = 00000000, 0=00000000, --- = 0000000000000000
100 = 00000000, 0=00000000, --- = 0000000000000000
100 = 00000000, 0=00000000, --- = 0000000000000000
100 = 00000000, 0=00000000, --- = 0000000000000000
```

(c gives the multiplication of a and b)



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Table of Contents Vedic Multiplier Verilog Code

1. Understanding the eBook Vedic Multiplier Verilog Code
 - The Rise of Digital Reading Vedic Multiplier Verilog Code
 - Advantages of eBooks Over Traditional Books
2. Identifying Vedic Multiplier Verilog Code
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Vedic Multiplier Verilog Code
 - User-Friendly Interface
4. Exploring eBook Recommendations from Vedic Multiplier Verilog Code
 - Personalized Recommendations
 - Vedic Multiplier Verilog Code User Reviews and Ratings

- Vedic Multiplier Verilog Code and Bestseller Lists
- 5. Accessing Vedic Multiplier Verilog Code Free and Paid eBooks
 - Vedic Multiplier Verilog Code Public Domain eBooks
 - Vedic Multiplier Verilog Code eBook Subscription Services
 - Vedic Multiplier Verilog Code Budget-Friendly Options
- 6. Navigating Vedic Multiplier Verilog Code eBook Formats
 - ePub, PDF, MOBI, and More
 - Vedic Multiplier Verilog Code Compatibility with Devices
 - Vedic Multiplier Verilog Code Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Vedic Multiplier Verilog Code
 - Highlighting and Note-Taking Vedic Multiplier Verilog Code
 - Interactive Elements Vedic Multiplier Verilog Code
- 8. Staying Engaged with Vedic Multiplier Verilog Code
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Vedic Multiplier Verilog Code
- 9. Balancing eBooks and Physical Books Vedic Multiplier Verilog Code
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Vedic Multiplier Verilog Code
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Vedic Multiplier Verilog Code
 - Setting Reading Goals Vedic Multiplier Verilog Code
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Vedic Multiplier Verilog Code
 - Fact-Checking eBook Content of Vedic Multiplier Verilog Code
 - Distinguishing Credible Sources

13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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