Mohammad Tehranipoor · Ke Peng
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Test and Diagnosis for Small-Delay Defects

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Test And Diagnosis For Small Delay Defects

Ke Peng

Test And Diagnosis For Small Delay Defects:

Test and Diagnosis for Small-Delay Defects Mohammad Tehranipoor,Ke Peng,Krishnendu Chakrabarty,2011-09-08 This book will introduce new techniques for detecting and diagnosing small delay defects in integrated circuits Although this sort of timing defect is commonly found in integrated circuits manufactured with nanometer technology this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small delay defects including important parameters such as process variations crosstalk and power supply noise **High-quality Test and Diagnosis for Small-delay Defects** Ke Peng,2010 *Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits* Sandeep K. Goel,Krishnendu Chakrabarty,2017-12-19 Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits ICs However the increased complexity and nanometer size features of modern ICs make them susceptible to manufacturing defects as well as performance and quality issues Testing for Small Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations power supply noise crosstalk resistive opens bridges and design for manufacturing DfM related rule violations The book also addresses testing for small delay defects SDDs which can cause immediate timing failures on both critical and non critical paths in the circuit Overviews semiconductor industry test challenges and the need for SDD testing including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on alternative methods that explores new metrics top off ATPG and circuit topology based solutions Highlights the advantages and disadvantages of a diverse set of metrics and identifies scope for improvement Written from the triple viewpoint of university researchers EDA tool developers and chip designers and tool users this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective The book is designed as a one stop reference for current industrial practices research challenges in the domain of SDD testing and recent developments in SDD solutions

Machine Learning Support for Fault Diagnosis of System-on-Chip Patrick Girard,Shawn Blanton,Li-C. Wang,2023-03-13 This book provides a state of the art guide to Machine Learning ML based techniques that have been shown to be highly efficient for diagnosis of failures in electronic circuits and systems The methods discussed can be used for volume diagnosis after manufacturing or for diagnosis of customer returns Readers will be enabled to deal with huge amount of insightful test data that cannot be exploited otherwise in an efficient timely manner After some background on fault diagnosis and machine learning the authors explain and apply optimized techniques from the ML domain to solve the fault diagnosis problem in the realm of electronic system design and manufacturing These techniques can be used for failure isolation in logic or analog circuits board level fault diagnosis or even wafer level failure cluster identification Evaluation metrics as well as industrial case studies are used to emphasize the usefulness and benefits of using ML based diagnosis techniques **Hardware Security** Mark Tehranipoor,Kimia Zamiri Azar,Navid Asadizanjani,Fahim Rahman,Hadi Mardani

Kamali,Farimah Farahmandi,2024-06-11 This book provides a look into the future of hardware and microelectronics security with an emphasis on potential directions in security aware design security verification and validation building trusted execution environments and physical assurance The book emphasizes some critical questions that must be answered in the domain of hardware and microelectronics security in the next 5 10 years i The notion of security must be migrated from IP level to system level ii What would be the future of IP and IC protection against emerging threats iii How security solutions could be migrated expanded from SoC level to SiP level iv the advances in power side channel analysis with emphasis on post quantum cryptography algorithms v how to enable digital twin for secure semiconductor lifecycle management and vi how physical assurance will look like with considerations of emerging technologies The main aim of this book is to serve as a comprehensive and concise roadmap for new learners and educators navigating the evolving research directions in the domain of hardware and microelectronic securities Overall throughout 11 chapters the book provides numerous frameworks countermeasures security evaluations and roadmaps for the future of hardware security Resilient Computer System Design Victor Castano,Igor Schagaev,2015-04-15 This book presents a paradigm for designing new generation resilient and evolving computer systems including their key concepts elements of supportive theory methods of analysis and synthesis of ICT with new properties of evolving functioning as well as implementation schemes and their prototyping The book explains why new ICT applications require a complete redesign of computer systems to address challenges of extreme reliability high performance and power efficiency The authors present a comprehensive treatment for designing the next generation of computers especially addressing safety critical autonomous real time military banking and wearable health care systems

System-on-Chip Test Architectures Laung-Terng Wang,Charles E. Stroud,Nur A. Touba,2010-07-28 Modern electronics testing has a legacy of more than 40 years The introduction of new technologies especially nanometer technologies with 90nm or smaller geometry has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers As a result semiconductor test costs have been growing steadily and typically amount to 40% of today s overall product cost This book is a comprehensive guide to new VLSI Testing and Design for Testability techniques that will allow students researchers DFT practitioners and VLSI designers to master quickly System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations examples Most up to date coverage available including Fault Tolerance Low Power Testing Defect and Error Tolerance Network on Chip NOC Testing Software Based Self Testing FPGA Testing MEMS Testing and System In Package SIP Testing which are not yet available in any testing book Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits Discusses future nanotechnology test trends and challenges facing the nanometer design era promising nanotechnology test techniques including Quantum Dots

Cellular Automata Carbon Nanotubes and Hybrid Semiconductor Nanowire Molecular Computing Practical problems at the end of each chapter for students *Test Generation of Crosstalk Delay Faults in VLSI Circuits* S. Jayanthy,M.C. Bhuvaneswari,2018-09-20 This book describes a variety of test generation algorithms for testing crosstalk delay faults in VLSI circuits It introduces readers to the various crosstalk effects and describes both deterministic and simulation based methods for testing crosstalk delay faults The book begins with a focus on currently available crosstalk delay models test generation algorithms for delay faults and crosstalk delay faults before moving on to deterministic algorithms and simulation based algorithms used to test crosstalk delay faults Given its depth of coverage the book will be of interest to design engineers and researchers in the field of VLSI Testing **Nanometer Technology Designs** Nisar Ahmed,2010-02-26 Adopting new fabrication technologies not only provides higher integration and enhances performance but also increases the types of manufacturing defects With design size in millions of gates and working frequency in GHz timing related defects havv become a high proportion of the total chip defects For nanometer technology designs the stuck at fault test alone cannot ensure a high quality level of chips At speed tests using the transition fault model has become a requirement in technologies below 180nm Traditional at speed test methods cannot guarantee high quality test results as they face many new challenges Supply noise including IR drop ground bounce and Ldi dt effects on chip performance high test pattern volume low fault defect coverage small delay defect test pattern generation high cost of test implementation and application and utilizing low cost testers are among these challenges This book discusses these challenges in detail and proposes new techniques and methodologies to improve the overall quality of the transition fault test **Models in Hardware Testing** Hans-Joachim Wunderlich,2009-11-12 Model based testing is the most powerful technique for testing hardware and software systems Models in Hardware Testing describes the use of models at all the levels of hardware testing The relevant fault models for nanoscaled CMOS technology are introduced and their implications on fault simulation automatic test pattern generation fault diagnosis memory testing and power aware testing are discussed Models and the corresponding algorithms are considered with respect to the most recent state of the art and they are put into a historical context by a concluding chapter on the use of physical fault models in fault tolerance *ISTFA 2013* A. S. M. International,2013-01-01 This volume features the latest research and practical data from the premier event for the microelectronics failure analysis community The papers cover a wide range of testing and failure analysis topics of practical value to anyone working to detect understand and eliminate electronic device and system failures *Built-in Fault-Tolerant Computing Paradigm for Resilient Large-Scale Chip Design* Xiaowei Li,Guihai Yan,Cheng Liu,2023-03-01 With the end of Dennard scaling and Moore s law IC chips especially large scale ones now face more reliability challenges and reliability has become one of the mainstay merits of VLSI designs In this context this book presents a built in on chip fault tolerant computing paradigm that seeks to combine fault detection fault diagnosis and error recovery in large scale VLSI design in a unified manner so as to minimize resource

overhead and performance penalties Following this computing paradigm we propose a holistic solution based on three key components self test self diagnosis and self repair or 3S for short We then explore the use of 3S for general IC designs general purpose processors network on chip NoC and deep learning accelerators and present prototypes to demonstrate how 3S responds to in field silicon degradation and recovery under various runtime faults caused by aging process variations or radical particles Moreover we demonstrate that 3S not only offers a powerful backbone for various on chip fault tolerant designs and implementations but also has farther reaching implications such as maintaining graceful performance degradation mitigating the impact of verification blind spots and improving chip yield This book is the outcome of extensive fault tolerant computing research pursued at the State Key Lab of Processors Institute of Computing Technology Chinese Academy of Sciences over the past decade The proposed built in on chip fault tolerant computing paradigm has been verified in a broad range of scenarios from small processors in satellite computers to large processors in HPCs Hopefully it will provide an alternative yet effective solution to the growing reliability challenges for large scale VLSI designs ISTFA 2012 ASM International,EDFAS Organizing Committee, editors,2012 Hardware Security Swarup Bhunia,Mark M. Tehranipoor,2018-10-30 Hardware Security A Hands On Learning Approach provides a broad comprehensive and practical overview of hardware security that encompasses all levels of the electronic hardware infrastructure It covers basic concepts like advanced attack techniques and countermeasures that are illustrated through theory case studies and well designed hands on laboratory exercises for each key concept The book is ideal as a textbook for upper level undergraduate students studying computer engineering computer science electrical engineering and biomedical engineering but is also a handy reference for graduate students researchers and industry professionals For academic courses the book contains a robust suite of teaching ancillaries Users will be able to access schematic layout and design files for a printed circuit board for hardware hacking i e the HaHa board that can be used by instructors to fabricate boards a suite of videos that demonstrate different hardware vulnerabilities hardware attacks and countermeasures and a detailed description and user manual for companion materials Provides a thorough overview of computer hardware including the fundamentals of computer systems and the implications of security risks Includes discussion of the liability safety and privacy implications of hardware and software security and interaction Gives insights on a wide range of security trust issues and emerging attacks and protection mechanisms in the electronic hardware lifecycle from design fabrication test and distribution straight through to supply chain and deployment in the field A full range of instructor and student support materials can be found on the authors own website for the book http hwsecuritybook org **Introduction to Hardware Security and Trust** Mohammad Tehranipoor,Cliff Wang,2011-09-22 This book provides the foundations for understanding hardware security and trust which have become major concerns for national security over the past decade Coverage includes security and trust issues in all types of electronic devices and systems such as ASICs COTS FPGAs microprocessors DSPs and embedded systems This

serves as an invaluable reference to the state of the art research that is of critical significance to the security of and trust in modern society s microelectronic supported infrastructures VLSI Test Principles and Architectures Laung-Terng Wang,Cheng-Wen Wu,Xiaoqing Wen,2006-08-14 This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product drive down test cost improve product quality and yield and speed up time to market and time to volume Most up to date coverage of design for testability Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books Numerous practical examples in each chapter illustrating basic VLSI test principles and DFT architectures Testing of Interposer-Based 2.5D Integrated Circuits Ran Wang,Krishnendu Chakrabarty,2017-03-20 This book provides readers with an insightful guide to the design testing and optimization of 2 5D integrated circuits The authors describe a set of design for test methods to address various challenges posed by the new generation of 2 5D ICs including pre bond testing of the silicon interposer at speed interconnect testing built in self test architecture extest scheduling and a programmable method for low power scan shift in SoC dies This book covers many testing techniques that have already been used in mainstream semiconductor companies Readers will benefit from an in depth look at test technology solutions that are needed to make 2 5D ICs a reality and commercially viable *Asian Test Symposium* ,2005 *Delay Fault Testing for VLSI Circuits* Angela Krstic,Kwang-Ting (Tim) Cheng,2012-12-06 In the early days of digital design we were concerned with the logical correctness of circuits We knew that if we slowed down the clock signal sufficiently the circuit would function correctly With improvements in the semiconductor process technology our expectations on speed have soared A frequently asked question in the last decade has been how fast can the clock run This puts significant demands on timing analysis and delay testing Fueled by the above events a tremendous growth has occurred in the research on delay testing Recent work includes fault models algorithms for test generation and fault simulation and methods for design and synthesis for testability The authors of this book Angela Krstic and Tim Cheng have personally contributed to this research Now they do an even greater service to the profession by collecting the work of a large number of researchers In addition to expounding such a great deal of information they have delivered it with utmost clarity To further the reader s understanding many key concepts are illustrated by simple examples The basic ideas of delay testing have reached a level of maturity that makes them suitable for practice In that sense this book is the best x DELAY FAULT TESTING FOR VLSI CIRCUITS available guide for an engineer designing or testing VLSI systems Tech niques for path delay testing and for use of slower test equipment to test high speed circuits are of particular interest **Electronic Design Automation for IC System Design, Verification, and Testing** Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-12-19 The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logic verification and testing Chapters contributed by leading experts

authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for integrated circuit IC designs design and verification languages digital simulation hardware acceleration and emulation and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on high level synthesis system on chip SoC block based design and back annotating system level models Offering improved depth and modernity Electronic Design Automation for IC System Design Verification and Testing provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals

The book delves into Test And Diagnosis For Small Delay Defects. Test And Diagnosis For Small Delay Defects is a vital topic that must be grasped by everyone, ranging from students and scholars to the general public. This book will furnish comprehensive and in-depth insights into Test And Diagnosis For Small Delay Defects, encompassing both the fundamentals and more intricate discussions.

1. The book is structured into several chapters, namely:
    - Chapter 1: Introduction to Test And Diagnosis For Small Delay Defects
    - Chapter 2: Essential Elements of Test And Diagnosis For Small Delay Defects
    - Chapter 3: Test And Diagnosis For Small Delay Defects in Everyday Life
    - Chapter 4: Test And Diagnosis For Small Delay Defects in Specific Contexts
    - Chapter 5: Conclusion
2. In chapter 1, the author will provide an overview of Test And Diagnosis For Small Delay Defects. The first chapter will explore what Test And Diagnosis For Small Delay Defects is, why Test And Diagnosis For Small Delay Defects is vital, and how to effectively learn about Test And Diagnosis For Small Delay Defects.
3. In chapter 2, the author will delve into the foundational concepts of Test And Diagnosis For Small Delay Defects. This chapter will elucidate the essential principles that need to be understood to grasp Test And Diagnosis For Small Delay Defects in its entirety.
4. In chapter 3, this book will examine the practical applications of Test And Diagnosis For Small Delay Defects in daily life. This chapter will showcase real-world examples of how Test And Diagnosis For Small Delay Defects can be effectively utilized in everyday scenarios.
5. In chapter 4, the author will scrutinize the relevance of Test And Diagnosis For Small Delay Defects in specific contexts. This chapter will explore how Test And Diagnosis For Small Delay Defects is applied in specialized fields, such as education, business, and technology.
6. In chapter 5, the author will draw a conclusion about Test And Diagnosis For Small Delay Defects. This chapter will summarize the key points that have been discussed throughout the book.
   This book is crafted in an easy-to-understand language and is complemented by engaging illustrations. It is highly recommended for anyone seeking to gain a comprehensive understanding of Test And Diagnosis For Small Delay Defects.

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Test And Diagnosis For Small Delay Defects Introduction

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