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Documentation

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Using Altium Designer Rtl Guide Visual Basic

Douglas E. Ott, Thomas J. Wilderotter



Using Altium Designer Rtl Guide Visual Basic:

A Designer's Guide to VHDL Synthesis Douglas E. Ott, Thomas J. Wilderotter, 2013-12-19 A Designer's Guide to VHDL Synthesis is intended for both design engineers who want to use VHDL based logic synthesis ASICs and for managers who need to gain a practical understanding of the issues involved in using this technology The emphasis is placed more on practical applications of VHDL and synthesis based on actual experiences rather than on a more theoretical approach to the language VHDL and logic synthesis tools provide very powerful capabilities for ASIC design but are also very complex and represent a radical departure from traditional design methods This situation has made it difficult to get started in using this technology for both designers and management since a major learning effort and culture change is required A Designer's Guide to VHDL Synthesis has been written to help design engineers and other professionals successfully make the transition to a design methodology based on VHDL and log synthesis instead of the more traditional schematic based approach While there are a number of texts on the VHDL language and its use in simulation little has been written from a designer's viewpoint on how to use VHDL and logic synthesis to design real ASIC systems The material in this book is based on experience gained in successfully using these techniques for ASIC design and relies heavily on realistic examples to demonstrate the principles involved

Principles of VLSI RTL Design Sanjay Churiwala, Sapan Garg, 2011-05-04 Since register transfer level RTL design is less about being a bright engineer and more about knowing the downstream implications of your work this book explains the impact of design decisions taken that may give rise later in the product lifecycle to issues related to testability data synchronization across clock domains synthesizability power consumption routability etc all which are a function of the way the RTL was originally written Readers will benefit from a highly practical approach to the fundamentals of these topics and will be given clear guidance regarding necessary safeguards to observe during RTL design

SystemVerilog for Design Second Edition Stuart Sutherland, Simon Davidmann, Peter Flake, 2006-09-15 SystemVerilog is a rich set of extensions to the IEEE 1364 2001 Verilog Hardware Description Language Verilog HDL These extensions address two major aspects of HDL based design First modeling very large designs with concise accurate and intuitive code Second writing high level test programs to efficiently and effectively verify these large designs The first edition of this book addressed the first aspect of the SystemVerilog extensions to Verilog Important modeling features were presented such as two state data types enumerated types user defined types structures unions and interfaces Emphasis was placed on the proper usage of these enhancements for simulation and synthesis SystemVerilog for Design Second Edition has been extensively revised on a chapter by chapter basis to include the many text and example updates needed to reflect changes that were made between the first edition of this book was written and the finalization of the new standard It is important that the book reflect these syntax and semantic changes to the SystemVerilog language In addition the second edition features a new chapter that explains the SystemVerilog packages a new appendix that summarizes the synthesis guidelines presented

throughout the book and all of the code examples have been updated to the final syntax and rerun using the latest version of the Synopsys Mentor and Cadance tools High-Level Synthesis Blue Book Michael Fingeroff,2010-09 High Level Synthesis Blue Book is now available in Japanese This is the Japanese version of the book Are you an RTL or system designer that is currently using moving or planning to move to an HLS design environment Finally a comprehensive guide for designing hardware using C is here Michael Fingeroff s High Level Synthesis Blue Book presents the most effective C synthesis coding style for achieving high quality RTL Master a totally new design methodology for coding increasingly complex designs This book provides a step by step approach to using C as a hardware design language including an introduction to the basics of HLS using concepts familiar to RTL designers Each chapter provides easy to understand C examples along with hardware and timing diagrams where appropriate The book progresses from simple concepts such as sequential logic design to more complicated topics such as memory architecture and hierarchical sub system design Later chapters bring together many of the earlier HLS design concepts through their application in simplified design examples These examples illustrate the fundamental principles behind C hardware design which will translate to much larger designs Although this book focuses primarily on C and C to present the basics of C synthesis all of the concepts are equally applicable to SystemC when describing the core algorithmic part of a design On completion of this book readers should be well on their way to becoming experts in high level synthesis

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