

CBGS SCHEME

USN

18EC72

Seventh Semester B.E. Degree Examination, Feb./Mar. 2022 VLSI Design

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. With necessary circuit diagram, explain the operation of tristate inverter. Also realize a 2 : 1 multiplexer using tristate inverter. (08 Marks)
- b. Implement a D flip-flop using transmission gates and explain its operation with necessary timing diagram. (08 Marks)
- c. Realize CMOS compound gate for the function $Y = \overline{A(B+C)} + DE$. (04 Marks)

OR

- 2 a. Explain the operation of MOSFET with necessary diagrams. Also derive the equation for drain current in linear and saturation region of operation. (10 Marks)
- b. Draw the circuit of CMOS inverter and explain its DC transfer characteristics. (06 Marks)
- c. Explain the following non-ideal effects channel length modulation, mobility degradation. (04 Marks)

Module-2

- 3 a. Explain CMOS n-well fabrication process with necessary diagrams. (12 Marks)
- b. What is scaling. Compute drain current, power, current density and power density for constant field and constant voltage scaling. (08 Marks)

OR

- 4 a. Draw the layout of $Y = \overline{(A+B+C)}D$ and estimate the area. (08 Marks)
- b. Mention different types of MOSFET capacitances and explain with necessary diagrams and equations. (06 Marks)
- c. With neat diagram, explain lambda based design rules for wires and contacts. (06 Marks)

Module-3

- 5 a. Develop the RC delay model to compute the delay of the logic circuit and calculate the delay of unit sized inverter driving another unit inverter. (08 Marks)
- b. Explain Cascode Voltage Switch Logic (CVSL). Also realize two input AND/NAND using CVSL. (06 Marks)
- c. Explain linear delay model. Compare the logical efforts of the following gates with the help of schematic diagrams :
i) 2-input NAND gate ii) 3-input NOR gate. (06 Marks)

OR

- 6 a. Explain : i) pseudo nMOS ii) ganged CMOS with necessary circuit examples. (06 Marks)
- b. Estimate t_{par} and t_{ps} of a 3-input NAND gate if the output is loaded with h identical gates. Use Elmore delay model. (08 Marks)
- c. Explain clocked gates with an example. (06 Marks)

Vlsi Design Sixth Sem Question Paper

Jain Richa & Rai Amrita



Vlsi Design Sixth Sem Question Paper:

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